METHOD AND DEVICE FOR VERIFYING FREQUENCY OF CLOCK SIGNAL

ABSTRACT OF THE DISCLOSURE

A device for verifying frequency of a clock signal generated from a clock signal generator includes a reference signal generator, a frequency divider and a comparative detector. A reference clock signal and a reset signal are provided by the reference signal generator. The frequency divider in communication with the reference signal generator and the clock signal generator receives and frequency-divides the clock signal into a bi-level divided clock signal in response to the reset signal. Then the comparative detector in communication with the frequency divider and the reference signal generator detects a level of the bi-level divided clock signal in response to the reset signal and the reference clock signal, and verifies frequency of the clock signal according to a period deviation range Te when the bi-level divided clock signal is detected to be a first level from the first to the (p-q)th detected points but a second level at the (p+1)th detected point.